EXHIBIT 9

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,

Petitioner,

v.

NETLIST, INC.,

Patent Owner,

_____

Case No. IPR2022-00615

Patent No. 7,619,912

_____

REMOTE VIDEOTAPED DEPOSITION BY VIRTUAL ZOOM OF

ANDREW WOLFE, PH.D.

WEDNESDAY, JANUARY 4, 2023

Reported by:

Ashala Tylor, CSR #2436, CLR, CRR, RPR

JOB NO. 5621734

PAGES 1 - 233

something that could be implemented as a point-to-point link, but there's also a discussion of other kinds of links as well. 10:52

MR. CHANDLER: We have been going about two hours. Whenever you are at a good breaking point, it might be a nice time for a break. 10:52 10:53 10:53

MS. ZHONG: Sure. 10:53

Q. Why don't we take a look at your declaration, Exhibit 1003, page 77, paragraph 133. 10:53 10:53

Are you there? 10:53

A. Yes. 10:53

Q. So for the specific citation that you quoted here, which I believe we discussed earlier, that is a distinct signaling scheme from the JEDEC compliant signaling scheme; is that correct? 10:53 10:53 10:54 10:54

MR. CHANDLER: Objection. Form. 10:54

THE WITNESS: As I said, I'm not familiar off the top of my head with every JEDEC standard. But the particular example that's quoted in paragraph 133 that's from column 13, line 54, is describing something that's distinct from JESD21-C. 10:54 10:54 10:54 10:54 10:54

BY MS. ZHONG: 10:54

Q. So what's described -- what you quoted in paragraph 133 is a different signaling scheme than that is used for the RDIMM described in 10:54 10:54 10:54

MS. ZHONG: We can take a break. How long do you want it to be? 10:56 10:56

Why don't we get off the record and then we can discuss how long the breaks needs to be. 10:57 10:57

MR. CHANDLER: Okay. 10:57

(Recess.) 11:08

(Off record: 10:57 a.m.) 11:08

(On record: 11:16 a.m.) 11:08

MS. ZHONG: We can go back on the record. 11:16

Q. Dr. Wolfe, can you go back to your declaration, Exhibit 1003, page 93? 11:17 11:17

A. Okay. 11:17

Q. Do you see Table 10, the command truth table? 11:17 11:17

A. Yes. 11:17

Q. Is the content in that command truth table something that had a person of ordinary skill in the art would be familiar with at the time of the '912 inventions? 11:17 11:17 11:17 11:17

A. Yes. 11:18

Q. So, for example, they would know, for a DDR SDRAM, a write operation would include bank address information; is that correct? 11:18 11:18 11:18

A. Yes, for things that are compliant within JEDEC Standard 79-2. 11:18 11:18

Exhibit 1032; is that correct? 10:55

A. It is not an identical signaling mechanism, but it does have teachings that are applicable to the signaling mechanism used for DDR2. 10:55 10:55 10:55

Q. Okay. So, for example, it does not have the CS signal, the CAS, RAS -- let's go to page 16 of Exhibit 1032. 10:55 10:55 10:55

A. Uh-huh. 10:55

Q. For example, the signaling scheme described in 133 would not have the signals that's listed on the left-hand side of the register box; is that correct? 10:55 10:55 10:55 10:56

A. I think it would have those signals. It just wouldn't necessarily have them in the exact same physical form. It would have them in a way that has a different physical implementation. But certainly a person of ordinary skill in the art would understand how the teachings apply to both. 10:56 10:56 10:56 10:56 10:56 10:56

Q. Okay. So they will be a different physical implementation that's different than what's described on Exhibit 1032, page 16; is that right? 10:56 10:56 10:56

A. That's true with respect to that one particular statement. If you look at the teaching as a whole, it's broad enough to encompass what's in 1032. 10:56 10:56 10:56 10:56

Q. So they would know that in order for the SDRAM to perform a write operation the DIMM has to receive the bank address signals, correct? 11:18 11:18 11:18

A. Was the question that the DIMM has to receive the bank address signals? 11:18 11:18

Q. Correct. 11:18

A. That's from JESD79-2, which does not require a DIMM. But if that particular chip were on a DIMM, then the DIMM would need to receive the bank address signals. 11:19 11:19 11:19 11:19

Q. Okay. And so if a DDR or DDR2 device is on the DIMM, does that DIMM have to receive a bank address signal in order to perform a read operation? 11:19 11:19 11:19 11:19

A. If you're using a JEDEC Standard 79-2 memory on a DIMM, then that DIMM would need a bank address signal. 11:19 11:19 11:19

Q. Are you aware of DRAMs that do not use bank address signals for read or write operation? 11:19 11:19 11:19

A. Yes. 11:20

Q. Which kind of DRAMs do not use bank address signals for read and write operation? 11:20 11:20 11:20

A. I'd have to go back and look at the specific specifications. But, based on my recollection, perhaps the Burst EDO DRAMs may not have used them, or it may be a previous generation. 11:20 11:20 11:20 11:20

Q. Okay. What about DDR2, DDR SDRAMs? Are you aware of any such memory devices that do not use bank address signals for read or write operation?
A. If by DDR and DDR2 you mean things that are compliant with JESD79 or JESD79-2, in that case I'm not aware of any that don't use a bank address signal at the memory chip device itself. It doesn't necessarily have to be provided to anything else on the DIMM.
Q. So how can the bank address signals be provided to the SDRAM if the signal is not sent to the DIMM on which the SDRAM is sent on?
A. There are lots of different ways. You could do a design. You could generate them on the DIMM hypothetically, depending on what you were using the DIMM for and what you were trying to accomplish.
Q. Okay. So according to you, it is not necessary for DIMM to receive, for example, bank address signals, RAS, CAS -- let me withdraw and ask.
Is -- would it also be the case that for a read and write operation that's to be performed by a DDR, a DDR2 SDRAM, it is not necessary for the DIMM on which the SDRAM is set on to receive a chip

select signal?
A. It would not be necessary, but it would be ordinary for the DIMM to receive a chip select signal.
Q. And would it be ordinary for the DIMM to receive a bank address signal for a read and write operation?
A. If it were a memory DIMM that used memory chips compliant with JESD79 or JESD79-2, it would be ordinarily for that DIMM to be provided with a bank address signal. That bank address signal, in the simplest case, would go directly to the memory devices.
Q. What if it is a registered DIMM? Would that bank address signal go to the register on the DIMM side then?
A. Again, we'd have to look at the particular standards. But in the case of, for example, the JESD21-C registered DIMMs, bank address signals would go to a register typically.
Q. Were DDR2 or DDR SDRAMs common at the time of the '912 invention?
A. By "common" do you mean generally available?
Q. When someone says a DRAM device in 2004

and 2005, would the person of ordinary skill in the art that DDR2 -- (indiscernible.)
THE REPORTER: I'm sorry. Excuse me, Counsel. I lost you on that one. Repeat your question, please.
BY MS. ZHONG:
Q. So in 2004 and 2005, when a person with ordinary skill in the art mentions a DRAM device, would others understand that the DRAM device they refer to would include DDR2 or DDR device?
A. I think they would understand that it could include a DDR or DDR2 device, especially if they were in the context of a general purpose computer.
Q. Okay. And if the person -- the description for that DRAM device also include things such as chip select signals, would that also be consistent with the reference to a DDR or DDR2 device?
A. If I understand your question correctly, the use of chip select signals on a DDR or DDR2 memory device is ordinary.
Q. What do you mean by "ordinary"?
A. For the most commonly available devices would -- that are DDR or DDR2 in the 2004, 2005,

2006 time frame -- would be compliant with JESD79 or JESD79-2 and would include a chip select input.
Q. So if a DRAM device is described as including a chip select signal, would that indicate to a person of ordinary skill in the art that device is likely a DDR2 or DDR device?
A. No, that would generally not be a identifying or distinguishing characteristic.
Q. And you said that if the DRAM device was used in connection with a personal computer, then a person of ordinary skill in the art would understand that a DRAM device could be a DDR2 or DDR device, correct?
A. That would be true in the 2000 to 2006 time frame.
Q. Okay. And then they would understand that if those are DDR and DDR2 device, in order for the DDR -- in order for the memory device to perform a read, write, bank activation operation, it would be ordinary for the computer system to send signals such as bank address signals, chip select signals, CAS bar, RAS bar, and write enable bar; is that correct?
A. It would be ordinary to send those to an ordinary personal computer in DDR or DDR2 module at

that time. 11:30
Q. What do you mean by "It would be ordinary 11:30
to send those to an ordinary personal computer in 11:30
DDR or DDR2 module"? 11:30
A. One could -- one can use these chips in 11:30
many different ways and build many different kinds 11:30
of memory modules. But there were typical memory 11:30
modules at the time that were JEDEC compliant with 11:30
various JEDEC standards. 11:30
Q. Are you saying those CAS bar, RAS bar, WE, 11:30
and chip select and bank address signals are sent to 11:30
the personal computer instead of being sent from the 11:30
personal computer to the memory modules? 11:30
MR. CHANDLER: Vague. 11:31
THE WITNESS: No. 11:31
BY MS. ZHONG: 11:31
Q. Hello? 11:31
A. Yes. I answered, "no." 11:31
Q. You are saying that it would be ordinary 11:31
for a personal computer to send CAS bar, RAS bar, WE 11:31
bar, chip select signals and bank address signals to 11:31
the memory module for a read and write operation at 11:31
the time of the invention; is that correct? 11:31
A. Yes, I think that's fair. And then one 11:31
would have to look at how those are then connected 11:32

on the memory module to figure out whether or not 11:32
that's at all relevant to these claims. 11:32
Q. Is that something a person of ordinary 11:32
skill in the art would understand? 11:32
A. Yes. 11:32
Q. Can you pull up Exhibit 1034. 11:33
(Exhibit 1034 was marked for 11:33
identification and attached 11:33
hereto.) 11:33
THE WITNESS: Okay. 11:33
BY MS. ZHONG: 11:33
Q. Can you please go to page 2 of 11:33
Exhibit 1034. 11:33
A. Okay. 11:33
Q. The last paragraph on the right hand, 11:33
"disables the chip select bus." Do you see that? 11:33
A. Yes. 11:33
Q. So according to this paper, the chip 11:33
select bus is essential in the JEDEC-style memory 11:34
system. Do you agree with that? 11:34
A. In the context that's being used in this 11:34
paper where it's talking about DIMMs in a 11:34
traditional computer, I do think that the chip 11:34
select bus is essential in as far as it needs to 11:34
exist. 11:34

Q. In the Rambus memory module that you are 11:34
familiar with, there isn't a chip select bus; is 11:34
that correct? 11:34
A. There is not a distinct chip select bus. 11:34
It's subsumed into the -- into the Rambus channel. 11:34
Q. And what's your understanding of the chip 11:35
select bus in the context of Exhibit 1034? 11:35
A. I think that it's simply saying that in a 11:35
conventional PC-type memory system as of 2002 -- and 11:35
by "conventional," that's not the Rambus type -- 11:35
that there is a chip select signal provided for 11:35
every rank of memory in order to control the timing 11:35
of that rank with respect to responding to commands. 11:35
Q. So what's the difference between a bus 11:35
versus the point-to-point architecture described in 11:36
Perego? 11:36
A. A bus can be used broadly here. I think 11:36
in this particular reference, I think "bus" simply 11:36
is being used to refer to a collection of wires. 11:36
The -- again, and Perego does disclose 11:36
buses as alternatives to point-to-point. It 11:36
discloses both kinds of embodiments numerous times. 11:36
But in his point-to-point description in 11:36
Perego, he talks about things that have one 11:36
transceiver on each end, where in Perego buses used 11:36

a thing -- described things that can have more than 11:36
one transceiver. 11:36
I'm not sure that it's being used in 11:36
exactly the same way here. It's quite possible 11:36
that -- that this particular chip select bus the way 11:36
it would normally be implemented would be 11:36
point-to-point. 11:37
And it's also common to use the term "bus" 11:37
to simply refer to a collection of wires. And I 11:37
believe that's what's being done in 1034 in the area 11:37
that we referred to. 11:37
Q. Okay. So in the 2004 and 2005 time 11:37
period, a conventional PC system would send chip 11:37
select signals, CAS bar, RAS bar, write enable bar, 11:37
clock, bank address signals to a DIMM; is that 11:37
correct? 11:37
A. I don't know if it would send all of 11:37
those. 11:37
Q. Which signals you don't think it would 11:37
send? 11:38
A. I don't think it's just a clock at that 11:38
time frame. I think it tends to be a little more 11:38
complicated, and there are a number of -- 11:38
Q. Okay. 11:38
A. -- timing signals that are sent. 11:38